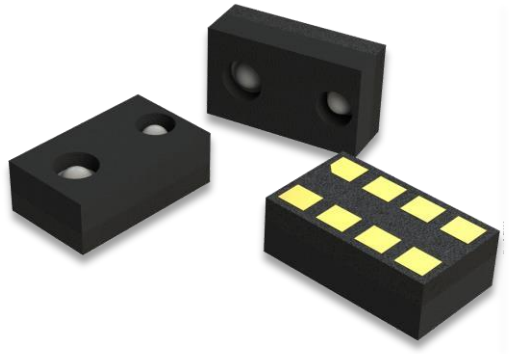
Digital ALS and Long Distance Proximity Sensor



Description

The WH4530A is a light to digital converter which combines an advanced ambient light sensor, an advanced proximity sensor and a high efficiency infra LED light.

Ambient light sensor (ALS) built-in an optical filter for IR rejection, and providing a spectrum which is close to the human eye's response. ALS can work from dark to direct sunlight, the selectable detect range is about 40dB. Dual-channel output (human eye and clear), so ALS has excellent light ratio under different light conditions.

Proximity sensor (PS) built-in an 940nm optical filter for ambient light immunity, so PS can detect reflected IR light with high precision and excellent rejection.

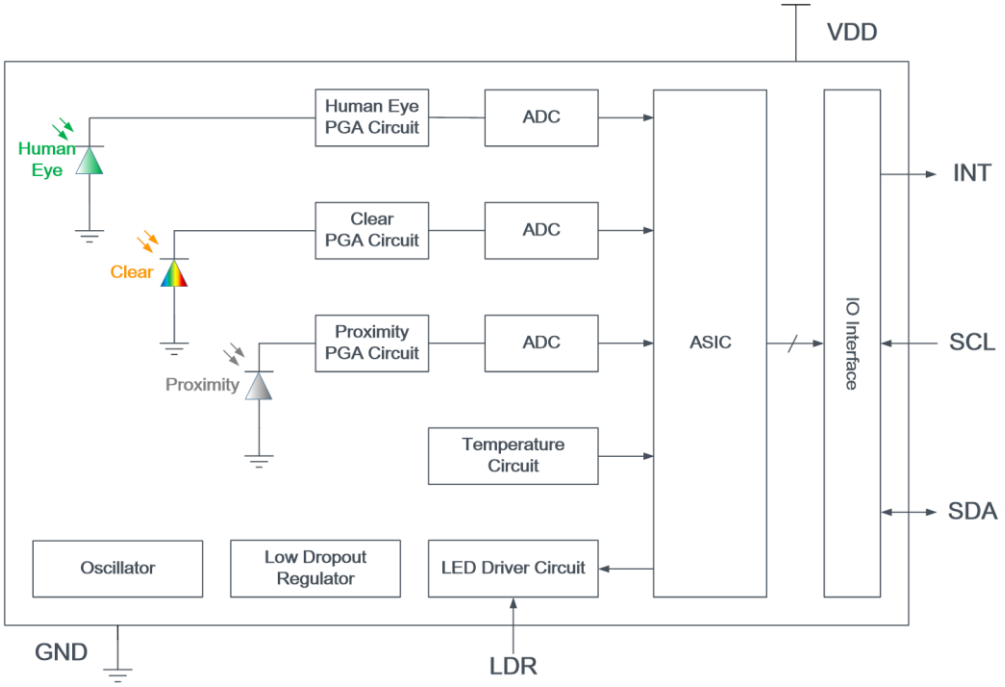
WH4530A has programmable interrupt function for ALS and PS with threshold based hysteresis.

Features

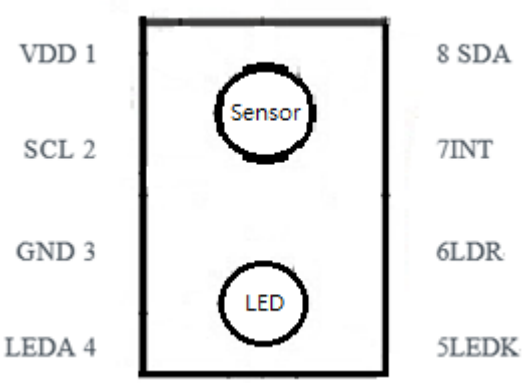
- I^2C interface (Fast Speed Mode at 400kHz/s)
- Supply voltage range from 2.4V to 3.6V
- Operating temperature from -40°C to +85°C
- Ambient Light Sensor
  - Spectral close to human eye response.
  - Fluorescent light flicker immunity.
  - Selectable gain and resolution (up to 16-bit).
  - High sensitivity and wide detect range.
  - High accuracy of illuminance & light ratio.
- Proximity Sensor
  - Recommended operating distance <100cm.
  - Selectable gain and resolution (up to 12-bit).
  - Programmable PWM and LED current.
  - Intelligent crosstalk calibration.
  - Speed mode for response time Improvement.

Applications

- Handset device
  Mobile phone, tablet, PDA, mobile POS
- Consumer device
  LCD TV, digital camera, toy
- Computing device
  Laptop, LCD monitor
- Smart home
  Smart lighting, smart curtain, night light
- Outdoor
  Surveillance system, street light
- Industrial Application



I/O Pins Configuration



Pin	I/O Type	Pin Name	Description
1		VDD	Power supply
2	I	SCL	I^2C serial clock line
3		GND	Ground
4		LEDA	LED anode
5		LEDK	LED cathode
6	O	LDR	LED driver
7	O	INT	Interrupt pin
8	I/O	SDA	I^2C serial data line

Absolute Maximum Ratings*

Parameter	Symbol	Value	Unit
Supply Voltage	VDD	4.5	V
I²C Bus Pin Voltage	SCL, SDA, INT	-0.2 to 4.5	V
I²C Bus Pin Current	SCL, SDA, INT	10	mA
LDR Pin Voltage	VLEDC, VLEDC	-0.2V to VDD + 0.5V	V
Operating Temperature	Tope	-40 to +85	˚C
Storage Temperature	Tstg	-45 to +100	˚C
ESD Rating	Human Body Model	2	KV

*Note: Exceeding these ratings could cause damage to the device. All voltages are with respect to ground. Currents are positive into, negative out of the specified terminal.

Recommended Operation Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Supply Voltage Note1	V_{DD}	2.4		3.6	V	
I²C Bus Pin Voltage	V_{Bus}	1.62	1.8	1.9	V	$V_{Bus} \leq V_{DD}$
Operating Temperature	T_{ope}	-40		+85	˚C	
I²C Bus Input High Voltage Note2	V_{IH_SCL}, V_{IH_SDA}	1.4			V	
I²C Bus Input Low Voltage Note2	V_{IL_SCL}, V_{IL_SDA}			0.5	V	
SDA Output Low Voltage	V_{OL_SDA}	0		0.4	V	3mA sinking current
		0		0.6	V	6mA sinking current
INT Output Low Voltage	V_{OL_INT}	0		0.4	V	3mA sinking current

Notes:

1. The power supply need to make sure the VDD slew rate at least 0.5V/ms. WH4530A have power on reset function. When VDD drops below 1.4V under room temp, the IC will be reset automatically. Then power back up at the requirement slew rate, and write registers to the desired values.
2. The specs are defined under VDD=3.3V, T=25°C

Electrical & Optical Specifications

Unless otherwise specified, the following specifications apply over the operating ambient temperature T=25˚C, VDD = 3.3V, and measure the output current by white light LED.

Electrical Characteristics	Symbol	MIN	TYP	MAX	Notes	Unit
Active Supply Current Note1	I_{DD}		160		Ev=0 Note1	μA
	I_{PD}		2.5		Sleep mode Ev= 0 I^2C inactive	μA
	I_{PD2}		1.5		Sleep mode Ev=0 EN_FRST = 1	μA
Device Boot Time Note2	T_{boot}		20			ms

ALS Characteristics Note3	Symbol	MIN	TYP	MAX	Notes	Unit
Sensing Gain, relative to x1 setting	**AGAIN**		4			
			8			
			32			
			96			
Unit of ADC integration time	AStep		2.66			ms
Number of ADC integration time	**ATIME**	1		256		AStep
Full ADC counts per step		0		1023	ATIME=1 AStep	count
Dark Count (White LED, Ev=0)	**ACH0**		1	3	AGAIN=96 ATIME=64	count
	ACH1		1	3	AGAIN=96 ATIME=64	count
Sensitivity (White LED, Ev=100Lux)	**ACH0**	19516	22960	26404	AGAIN=96 ATIME=64	Count
	ACH1	21760	25600	29440	AGAIN=96 ATIME=64	count

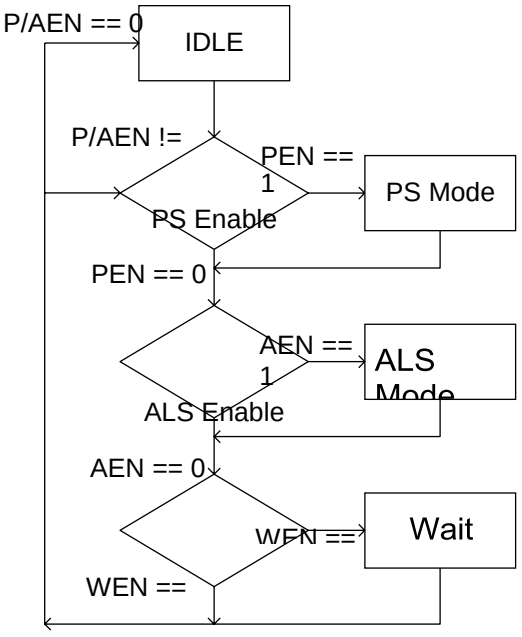
PS Characteristics	Symbol	MIN	TYP	MAX	Notes	Unit
Sensing Gain, relative to x1 setting	**PGAIN**		2			
			4			
			8			
Unit of ADC integration time	PStep		0.51			ms
Number of ADC integration time	**PTIME**	1		16		PStep
Full ADC counts per step		0		255		count
LED pulse period	T		13.8			μs
LED pulse count	**PLPUC**	1		256		pulse

LED Pulse width	**PLPUW**	1		64		T
LED Driving Current	**PLDR**		50		25%	mA
			100		50%	mA
			150		75%	mA
			200		100%	mA
IR Peak Wavelength			940			nm

Notes :
1. VDD = 3.3 V, TA = 25C, **EN_ALS**=1, **ATIME**=63, **AGAIN**=96, WTIME=8
2. The Device Boot Time (T_{boot}) is the delay time that the host can send the first I2C command after the VDD ready.

State Machine

There are two operation mode ALS and PS. The state machine is shown below:



Typical Characteristics Curves

Unless otherwise specified, the following specifications apply over the operating ambient temperature T = 25˚C, VDD = 3.3V.

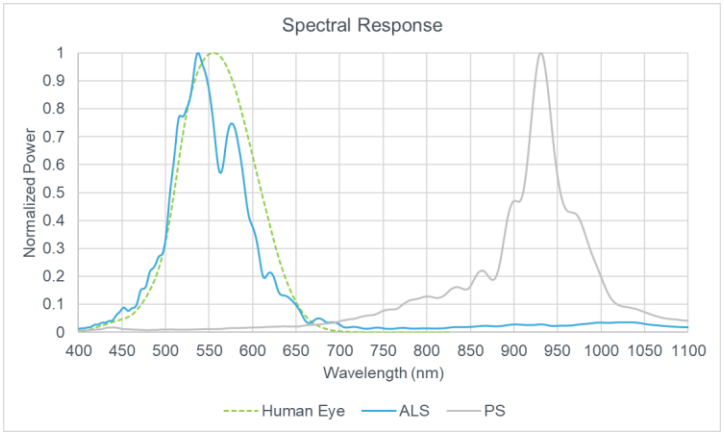


Fig. 2 ALS & PS Spectral Response

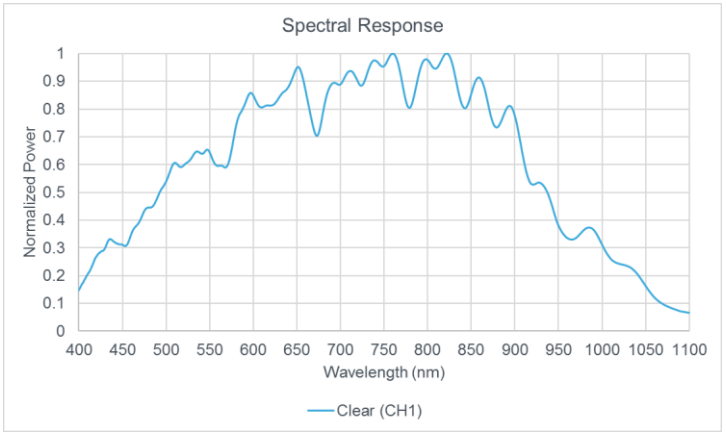


Fig. 3 Clear Spectral Response

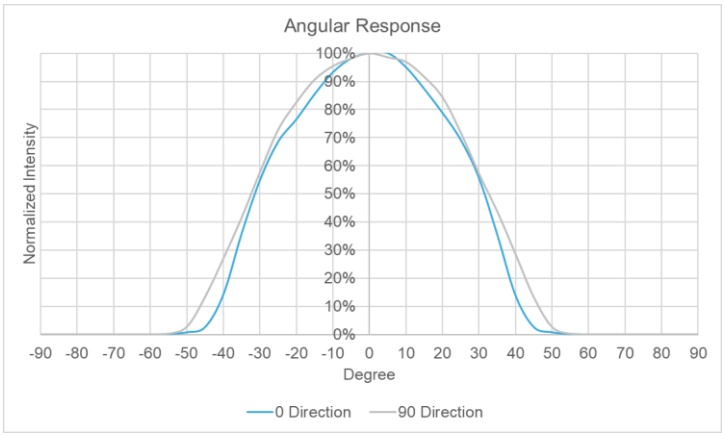


Fig. 4 ALS Angular Response

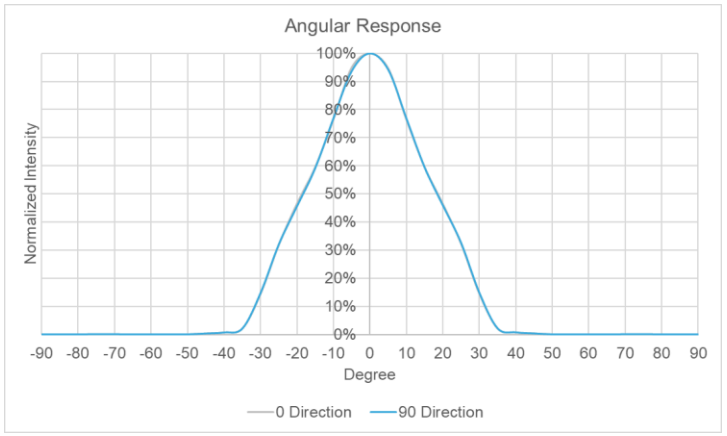


Fig. 5 LED Angular Response

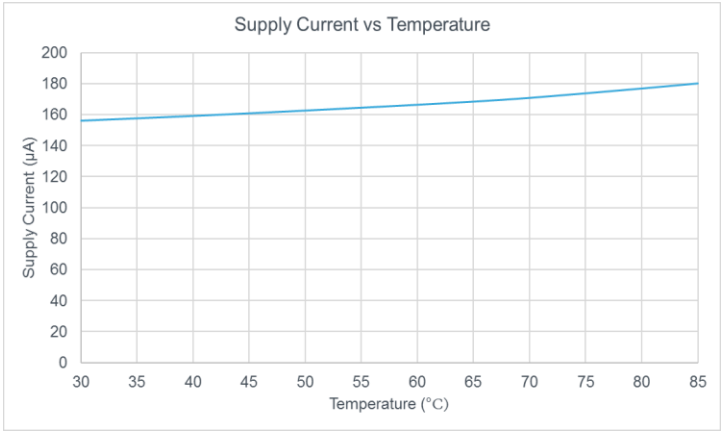
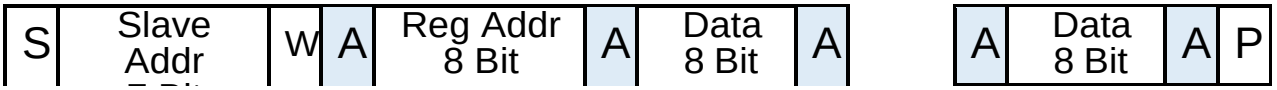


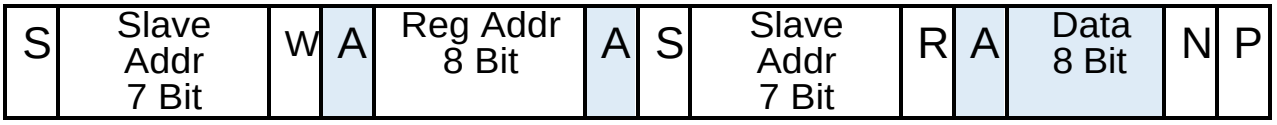
Fig. 6 Supply Current vs Temperature

I²C Write Format

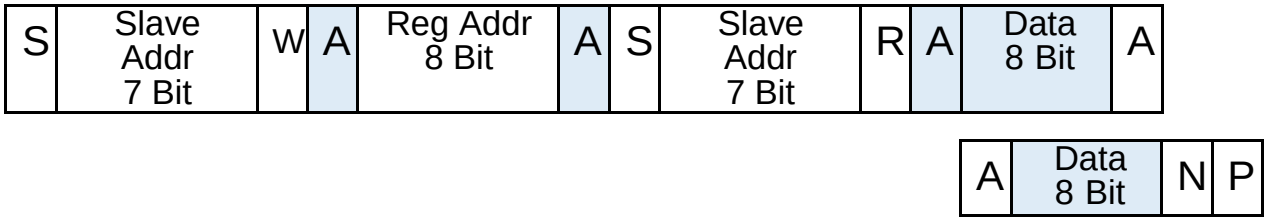
I²C Block Write Format



I²C Read Format



I²C Block Read Format



Master to Slave

Slave to Master

S Start Condition, 1 Bit

P Stop Condition, 1 Bit

W Write, Set 0 for write, 1 Bit

R Read, Set 1 for read, 1 Bit

A Acknowledge(ACK), Set 0, 1 Bit

N Non acknowledge(NACK), Set 1, 1 Bit

I²C Slave Address and R/W bit

This address is seven bits long followed by an eighth bit which is a data direction bit (R/W). A ‘0’ indicates a transmission (WRITE), a ‘1’ indicates a request for data (READ). The slave address of this device is 0x38.

Register Set

The WH4530A is operated over the I2C bus with registers that contain configuration, status, and result information. All registers are 8 bits long.

Address	Name	Type	Default value	Description
0x00	SYSM_CTRL	RW	0x00	ALS/PS operation mode control, waiting mode control, SW reset
0x01	INT_CTRL	RW	0x03	Interrupt pin control, interrupt persist control
0x02	INT_FLAG	RW	0x00	Interrupt flag, error flag, power on reset(POR) flag
0x03	WAIT_TIME	RW	0x00	Waiting time setting
0x04	ALS_GAIN	RW	0x00	ALS analog gain setting
0x05	ALS_TIME	RW	0x00	ALS integrated time setting
0x06	LED_CTRL	RW	0x00	LED setting
0x07	PS_GAIN	RW	0x00	PS analog gain setting
0x08	PS_PULSE	RW	0x00	PS number of LED pulse
0x09	PS_TIME	RW	0x00	PS integrated time setting
0x0B	PERSISTENCE	RW	0x11	ALS/PS persistence setting
0x0C	ALS_THRES_LL	RW	0x00	ALS lower interrupt threshold - LSB
0x0D	ALS_THRES_LH	RW	0x00	ALS lower interrupt threshold - MSB
0x0E	ALS_THRES_HL	RW	0xFF	ALS higher interrupt threshold - LSB
0x0F	ALS_THRES_HH	RW	0xFF	ALS higher interrupt threshold - MSB
0x10	PS_THRES_LL	RW	0x00	PS lower interrupt threshold - LSB
0x11	PS_THRES_LH	RW	0x00	PS lower interrupt threshold - MSB
0x12	PS_THRES_HL	RW	0xFF	PS higher interrupt threshold - LSB
0x13	PS_THRES_HH	RW	0xFF	PS higher interrupt threshold - MSB
0x14	PS_OFFSET_L	RW	0x00	PS offset level - LSB
0x15	PS_OFFSET_H	RW	0x00	PS offset level - MSB
0x16	INT_SOURCE	RW	0x00	ALS interrupt source
0x17	ERROR_FLAG	RW	0x00	Error flag
0x18	PS_DATA_L	R	0x00	PS output data - LSB
0x19	PS_DATA_H	R	0x00	PS output data - MSB
0x1A	IR_DATA_L	R	0x00	IR output data - LSB
0x1B	IR_DATA_H	R	0x00	IR output data - MSB
0x1C	CH0_DATA_L	R	0x00	Channel 0 output data - LSB
0x1D	CH0_DATA_H	R	0x00	Channel 0 output data - MSB
0x1E	CH1_DATA_L	R	0x00	Channel 1 output data - LSB

0x1F	CH1_DATA_H	R	0x00	Channel 1 output data - MSB

SYSM_CTRL

0x00	SYSM_CTRL, System Control (Default = 0x00)							
BIT	7	6	5	4	3	2	1	0
R/W	SWRST	EN_WAIT	EN_FRST	0	0	0	EN_PS	EN_ALS

SWRST：Software reset. Reset all register to default value.

0: (default)

1: Reset will be triggered.

EN_WAIT：Waiting time will be inserted between two measurements.

0: Disable waiting function.

1: Enable waiting function.

EN_FRST：Brown out detection function control

0: Disable

1: Enable

EN_PS：Enables PS function.

0: Disable PS function (default)

1: Enable PS function

EN_ALS：Enables ALS function.

0: Disable ALS function (default)

1: Enable ALS function

INT_CTRL

0x01	Interrupt Pin Control (Default = 0x03)							
BIT	7	6	5	4	3	2	1	0
R/W	PS_INT_ MODE	SINT_ MODE	PS_ SYNC	ALS_ SYNC	0	0	EN_PINT	EN_AINT

PS_INT_MODE ： This bit selects the interrupt triggered mode of PS function.

0: Hysteresis Mode (default).

1: Zone Mode.

SINT_MODE ： Speeding up the interrupt response of PS mode by skipping waiting time in each conversion cycle.

0: Disable speed up (default).

1: Enable speed up.

PS_SYNC ： Measurement is pended when PS interrupt is triggered. Until clear the interrupt then start the next measurement.

0: Disable pending PS function (default).

1: Enable pending PS function.

ALS_SYNC： Measurement is pended when ALS interrupt is triggered. Until clear the interrupt then start the next measurement.

0: Disable pending ALSfunction (default).

1: Enable pending ALS function.

EN_PINT ： The PS interrupt (INT_PS)flag can trigger the INT pin to low.

0: Disable **INT_PS** effect INT pin.

1: Enable **INT_PS** effect INT pin(default)

EN_AINT ： The ALS interrupt (INT_ALS)flag can trigger the INT pin to low.

0: Disable **INT_ALS** effect INT pin.

1: Enable **INT_ALS** effect INT pin(default)

INT_FLAG

0x02	INT_FLAG, System Control (Default = 0x00)							
BIT	7	6	5	4	3	2	1	0
R/W	INT_POR	DATA_FLAG	OBJ	0	0	0	INT_PS	INT_ALS

INT_POR：Power-On-Reset Interrupt flag trigger the INT pin when the flag sets to one. Write zero to clear the flag.

0:

1: This bit will be set to one when it satisfies one of the following conditions:

- Power On

- VDD < 1.4V
- SWRST

DATA_FLAG : It shows if any data is invalid after completion of each conversion cycle. This bit is read-only.

0: data valid

1: data invalid

OBJ：Object Detection Bit. It shows the position of the object. It is a read-only bit. Refer to **PMODE** (register 0x02, bit 5) for detailed definition of **OBJ**. This bit is read only.

0: object disappear.

1: object appear.

INT_PS : PS Interrupt flag. It correlation with **PS_INT_MODE.** PS_DATA and PS high/low threshold. Write zero to clear the flag.

0: PS Interrupt not triggered or be cleared.

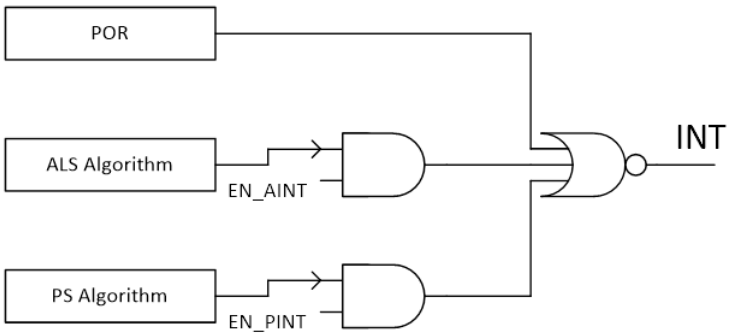
1: PS Interrupt triggered.

INT_ALS : ALS Interrupt flag. It correlation with CH0/1 data and ALS high/low threshold. Write zero to clear the flag.

0: ALS Interrupt not trigger or be cleared.

1: ALS Interrupt triggered

Interrupt Behavior :



ALS Interrupt Algorithm

Correlative register:

The ALS Interrupt (**INT_ALS, register 0x02, bit0).**

The ALS Persistence (**PRS_ALS**, register 0x0B, bit0 to bit3),

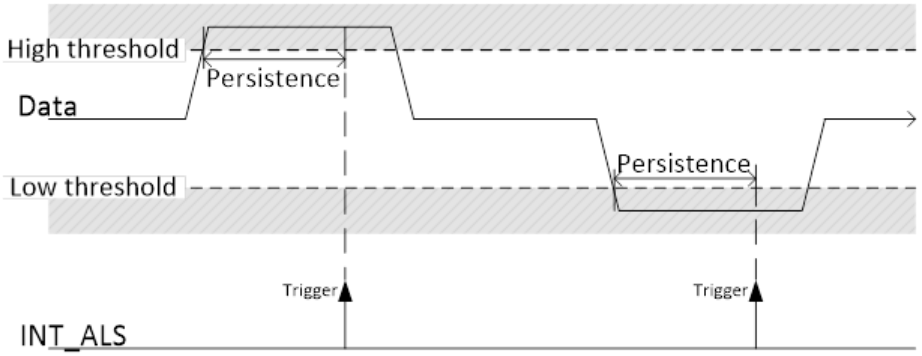
The ALS Data (**CH0_DATA and CH1_DATA**, register 0x1C to 0x1F),

The ALS Low Threshold (**ALS_THRES_L**, register 0x0C to 0x0D),

The ALS High Threshold (**ALS_THRES_H**, register 0x0E to 0x0F).

INT_ALS triggered condition:

1. Rule of active interrupt: **DATA**>**ALS_THRES_H** or **DATA**<**ALS_THRES_L.**
2. If the **DATA** meets the rule, the **interrupt** count increases one.
   If the **DATA** fails in the rule, the interrupt count will be clear.
3. When the **interrupt** count equal to **PRS_ALS setting**, **INT_ALS** will be triggered and reset the interrupt counter.
4. If **PRS_ALS** is set to zero, **threshold** will be ignored and **DATA** will meets the active interrupt rule forcibly.



PS Interrupt Algorithm

Correlative register:

The PS Interrupt (**INT_PS**, register 0x02, bit1),

The PS Persistence (**PRS_PS**, register 0x0B, bit4 to bit7),

The PS Data (**PS_DATA**, register 0x18 to 0x19),

The PS Low Threshold (**PS_THRES_L**, register 0x10 to 0x11),

The PS High Threshold (**PS_THRES_H**, register 0x12 to 0x13).

The PS Interrupt Mode (**PS_INT_MODE**, register 0x01, bit7).

PS_INT_MODE set to one: Zone Mode

INT_PS triggered condition:

1. Rule of active interrupt: **PS_DATA**>**PS_THRES_H** or **PS_DATA**<**PS_THRES_L**

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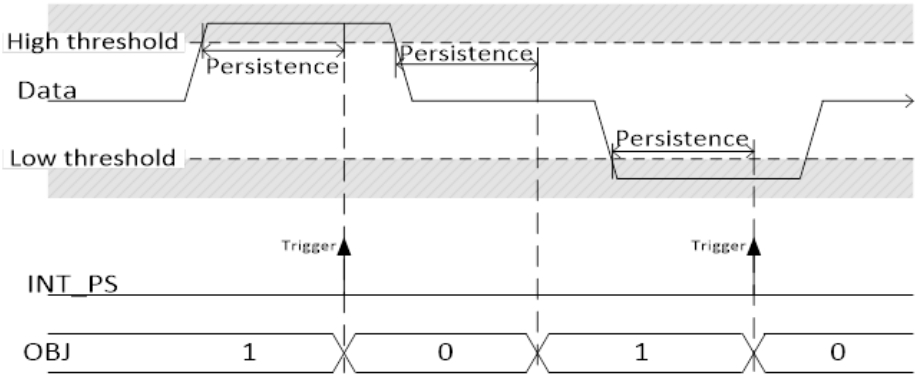
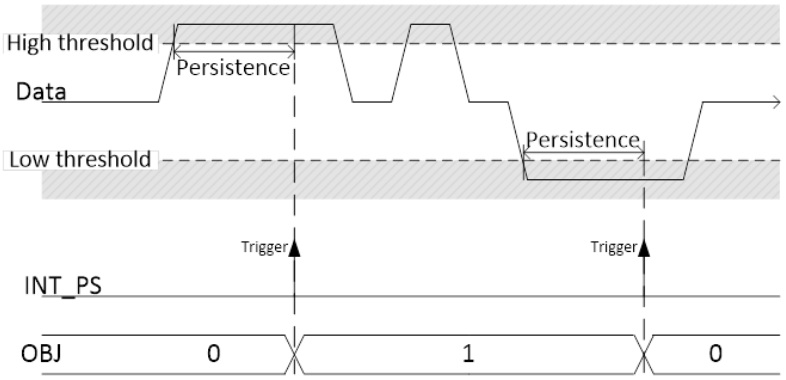
2. If **PS_DATA** meets the rule, the **counter (OUT_CONT)** increases one and another counter (**IN_CONT**) set to zero.
   If **PS_DATA** fails in the rule, the counter (**IN_CONT**) increases one and clear the value of **OUT_CONT**.
3. When the counter value of **OUT_CONT** equal to **PRS_PS**, the **OBJ** flag will set to zero, **INT_PS** will be triggered, and clear **OUT_CONT** counter.
   When the **IN_CONT** counter value reaches **PRS_PS**, the counter will be cleared and **OBJ** flag will set to one.
4. If **PRS_PS** is set to zero, **the threshold** setting will be ignored and **DATA** will meets the active interrupt rule forcibly



PS_INT_MODE set to zero: Hysteresis Interrupt mode:
INT_PS triggered condition:

1. Rule of active interrupt:
   i. When **OBJ** is zero, **PS_DATA**>**PS_THRES_H.**
   ii. **When OBJ** is one, **PS_DATA**<**PS_THRES_L.**
2. If **PS_DATA** meets the rule, the interrupt **counter** increases one.
   If **PS_DATA** fails in the rule, the interrupt counter will be cleared.
3. When the counter value equal to **PRS_PS**, the **OBJ** flag will be inverted, **INT_PS** will be triggered, and clear interrupt counter.
4. If **PRS_PS** is set to zero, **the threshold** setting will be ignored and **DATA** will meets the active interrupt rule forcibly.



WAIT_TIME

0x03	WAIT_TIME, waiting time (Default = 0x00)							
BIT	7	6	5	4	3	2	1	0
R/W	WTIME							

WTIME ： This register controls the time unit of waiting state which is inserted between any two measurements. It is 5ms per time unit.

0x00: 1 time unit.

0x01: 2 time units

……

0xFF: 256 time units

ALS_GAIN

0x04	ALS_GAIN, ALS analog gain (Default = 0x00)							
BIT	7	6	5	4	3	2	1	0
R/W	0	0	0	0	0	ALS_ RANGE	PGA_ALS	

ALS_RANGE ： Increase ALS sensing dynamic range (x96).

0: ALS gain is controlled by **PGA_ALS**(default).

1: ALS gain sets to external gain(x96).

PGA_ALS ： ALS sensing gain.

0x0: x1 (default)

0x1: x4

0x2: x8

0x3: x32

ALS_TIME

0x05	ALS_TIME, ALS integrated time (Default = 0x00)							
BIT	7	6	5	4	3	2	1	0
R/W	ALSCONV							

ALSCONV：This register controls the integrated time of AD converter at ALS mode (T_{ALS}), and the resolution of output data (CH0_DATA, CH1_DATA).

0x00: The maximum count of **output data is** 1023, T_{ALS} = 5.513ms (default)

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0x01: The maximum count of **output data is** 2047, T_{ALS} = 8.138ms

……

0xff: The maximum count of **output data is** 65535, T_{ALS} = 674.888ms

The maximum count of **output data is** minimum of [1024 x (**ATIME** + 1) – 1, 65535].

The conversion time of ALS function (T_{ALS}) is decided by **ALSCONV**.

T_{ALS}=2.888 + 2.625 x (**ALSCONV** + 1) (ms)

LED_CTRL

0x06	LED_CTRL, LED control(Default = 0x00)							
BIT	7	6	5	4	3	2	1	0
R/W	IRDR_SEL		ITW_PS					

IRDR_SEL：It configures the peak current of the internal LED driver.

0x00：50 mA

0x01：100 mA

0x02：150 mA 0x03：

200 mA (default)

ITW_PS：It controls the LED pulse width in PS function mode. Pulse width is 13.675us per unit.

0x00：1T, 13.675 us (default).

0x01：2T, 27.35 us.

…… 0x3F：

64T, 875.213 us.

PS_GAIN

0x07	PS_GAIN, PS analog gain (Default = 0x00)							
BIT	7	6	5	4	3	2	1	0
R/W	0	0	0	0	0	0	PGA_PS	

PGA_PS ：PS sensing gain.

0x0: x1 (default)

0x1: x2

0x2: x4

0x3: x8

PS_PULSE

0x08	PS_PULSE, PS pulse count control(Default = 0x00)							
BIT	7	6	5	4	3	2	1	0
R/W	ITC_PS							

ITC_PS：It controls the number of LED pulse in PS function mode.

0x00：1 pulse
0x01：2 pulses
0x02：3 pulses

……
0xFF：256 pulses

PS_TIME

0x09	PS_TIME, PS integrated time (Default = 0x00)							
BIT	7	6	5	4	3	2	1	0
R/W	0	0	0	0	PSCONV			

PSCONV：This register controls the integrated time of AD converter at PS mode (T_{PS}), and the resolution of output data (PS_DATA, IR_DATA).

0x0: The maximum count of **output data** is 255, 1 time unit (default).

0x1: The maximum count of **output data** is 511, 2 time units.

……

0xf: The maximum count of **output data** is 4095, 16 time units.

The maximum count of **output data** is 256 x (time unit -1).

The conversion time of PS function (T_{PS}) is decided by **ITW_PS**, **ITC_PS**, and **PSCONV**.

T_{PS} = [3.051 + (2 x **ITC_PS** + 1) x (0.01 + 0.01368 x **ITW_PS**) + 0.51 x **PSCONV** (ms)] *16

The total conversion time (T_{TOTAL}) of device is decided by T_{ALS}, T_{PS}, T_{wait}.

$T_{TOTAL} = T_{ALS} + T_{PS} + T_{wait}$ (ms)

PERSISTENCE

iSweek www.isweek.cn
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0x0B	PERSISTENCE, ALS, and PS persistence setting (Default = 0x00)							
BIT	7	6	5	4	3	2	1	0
R/W	PRS_PS				PRS_ALS			

PRS_ALS：This register sets the numbers of similar consecutive ALS interrupt events before the interrupt pin is triggered.

0x0: Every ALS conversion is done.

0x1: 1 ALS interrupt event is asserted.

……

0xf: 15 consecutive ALS interrupt events are asserted.

PRS_PS：This register sets the numbers of similar consecutive PS interrupt events before the interrupt pin is triggered.

0x0: Every PS conversion is done.

0x1: 1 PS interrupt event is asserted.

……

0xf: 15 consecutive PS interrupt events are asserted.

ALS_THRES_L

0x0C 0x0D	ALS_THRES_L, ALS low interrupt threshold (Default = 0x0000)							
BIT	7	6	5	4	3	2	1	0
R/W	ALS_THRE_LL							
R/W	ALS_THRE_LH							

This register sets the lower threshold value of ALS interrupt. The interrupt algorithm compares the selected ALS data and ALS threshold value.

ALS_THRE_LL：ALS lower interrupt threshold value, LSB. (Reg. 0x0C)
ALS_THRE_LH：ALS lower interrupt threshold value, MSB. (Reg. 0x0D)

ALS_THRES_H

0x0E 0x0F	ALS_THRES_H, ALS high interrupt threshold (Default = 0xFFFF)							
BIT	7	6	5	4	3	2	1	0
R/W	ALS_THRE_HL							
R/W	ALS_THRE_HH							

This register sets the high threshold value of ALS interrupt. The interrupt algorithm compares the selected ALS data and ALS threshold value.

ALS_THRE_HL：ALS high interrupt threshold value, LSB. (Reg. 0x0E)
ALS_THRE_HH：ALS high interrupt threshold value, MSB. (Reg. 0x0F)

PS_THRES_L

0x10 0x11	PS_THRES_L, PS low interrupt threshold (Default = 0x0000)							
BIT	7	6	5	4	3	2	1	0
R/W	PS_THRE_LL							
R/W	PS_THRE_LH							

This register sets the lower threshold value of PS interrupt. The interrupt algorithm compares the selected PS data and PS threshold value.

PS_THRE_LL：PS lower interrupt threshold value, LSB. (Reg. 0x10)

PS_THRE_LH：PS lower interrupt threshold value, MSB. (Reg. 0x11)

PS_THRES_H

0x12 0x13	PS_THRES_H, PS high interrupt threshold (Default = 0xFFFF)							
BIT	7	6	5	4	3	2	1	0
R/W	PS_THRE_HL							
R/W	PS_THRE_HH							

This register sets the high threshold value of PS interrupt. The interrupt algorithm compares the selected PS data and PS threshold value.

PS_THRE_HL：PS high interrupt threshold value, LSB. (Reg. 0x12)

PS_THRE_HH：PS high interrupt threshold value, MSB. (Reg. 0x13)

PS_OFFSET

0x14 0x15	PS_OFFSET, PS offset level (Default = 0x0000)							
BIT	7	6	5	4	3	2	1	0
R/W	PS_OFFSET_L							
R/W	PS_OFFSET_H							

This register used to calibrate the device's cross talk. The **PS_DATA** should be closed to zero with no object. The PS_OFFSE is subtracted from the measured data before it output to **PS_DATA**.

PS_OFFSET_L：PS high interrupt threshold value, LSB. (Reg. 0x14)

PS_OFFSET_H：PS high interrupt threshold value, MSB. (Reg. 0x15)

INT_SOURCE

0x16	INT_SOURCE, ALS interrupt source (Default = 0x00)							
BIT	7	6	5	4	3	2	1	0
R/W	0	0	0	0	0	0	0	INT_SRC

INT_SRC : This register sets to select the ALS data for the ALS Interrupt algorithm.

0x0: Select CH0_DATA.

0x1: Select CH1_DATA.

ERROR_FLAG

0x17	ERROR_FLAG, Error flag status							
BIT	7	6	5	4	3	2	1	0
R/W	0	0	0	0	ERR_IR	0	ERR_CH1	ERR_CH0

This register indicates the ALS / IR data status. If the ALS / IR data is outside of measurable range, the corresponding error flag (ERR_CH0, ERR_CH1, ERR_IR) will set to one. That also means the data is invalid.

PS_DATA

0x18 0x19	PS_DATA, PS output data.							
BIT	7	6	5	4	3	2	1	0
R/W	PS_DATA _L							
R/W	PS_DATA_H							

The PS conversion result is written into PS_DATA.

For insuring the data in the register comes the same measurement, the high byte data will be latched when the low byte data has been accessed until the high byte data has be read.

IR_DATA

0x1A 0x1B	IR_DATA, IR output data.							
BIT	7	6	5	4	3	2	1	0
R/W	IR_DATA_L							
R/W	IR_DATA_H							

The IR sensor result is written into IR_DATA when PS conversion is done.
For insuring the data in the register comes the same measurement, the high byte data will be latched when the low byte data has been accessed until the high byte data has be read.

CH0_DATA

0x1C 0x1D	CH0_DATA, Channel 0 output data.							
BIT	7	6	5	4	3	2	1	0
R/W	CH0_DATA_L							
R/W	CH0_DATA_H							

The channel 0 result of ALS sensor is written into CH0_DATA when ALS conversion is done.
For insuring the data in the register comes the same measurement, the high byte data will be latched when the low byte data has been accessed until the high byte data has be read.

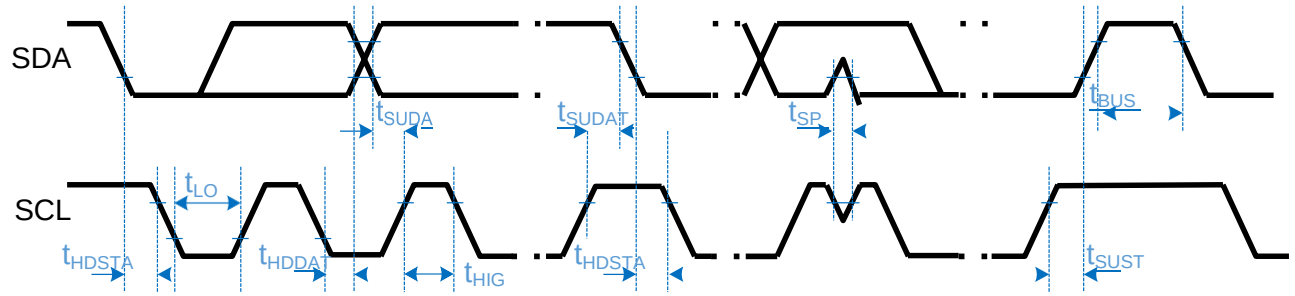
CH1_DATA

0x1E 0x1F	CH1_DATA, Channel 1 output data.							
BIT	7	6	5	4	3	2	1	0
R/W	CH1_DATA_L							
R/W	CH1_DATA_H							

The channel 1 result of ALS sensor is written into CH1_DATA when ALS conversion is done.
For insuring the data in the register comes the same measurement, the high byte data will be latched when the low byte data has been accessed until the high byte data has be read.

I²C Interface Timing Characteristics

This section will describe the protocol of the I²C bus. For more details and timing diagrams please refer to the I²C specification.



Parameter (*)	Symbol	Fast mode		Unit
		Min	Max	
SCL clock frequency	f_{SCL}	100	400	kHz
Bus free time between STOP condition and START condition	t_{BUS}	1.3	--	μs
LOW period of the SCL clock	t_{LOW}	1.3	--	μs
HIGH period of the SCL clock	t_{HIGH}	0.6	--	μs
Hold time (repeated) START condition	t_{HDSTA}	0.6	--	μs
Set-up time (repeated) START condition	t_{SUSTA}	0.6	--	μs
Set-up time for STOP condition	t_{SUSTO}	0.6	--	μs
Data hold time	t_{HDDAT}	50	--	ns
Data set-up time	t_{SUDAT}	100	--	ns
Pulse width of spikes which must be suppressed by the input filter	t_{SP}	0	50	ns
Rise time of both SDA and SCL signals		20 x VDD/5.5	300	ns
Fall time of both SDA and SCL signals		20 x VDD/5.5	300	ns

(*) Specified by design and characterization; not production tested.

(**) All specifications are at V_{Bus} = 3.3V, T_{ope}=25°C, unless otherwise noted.

Note:

I²CBus Clear

In the unlikely event where the clock (SCL) is stuck LOW, the preferential procedure is to reset the bus using the HW reset signal if your I2C devices have HW reset inputs. If theI2C devices do not have HW reset inputs, cycle power to the devices to activate the mandatory Internal Power-On Reset (POR) circuit.

If the data line (SDA) is stuck LOW, the master should send nine clock pulses. The device that held the bus LOW should release it sometime within those nine clocks.

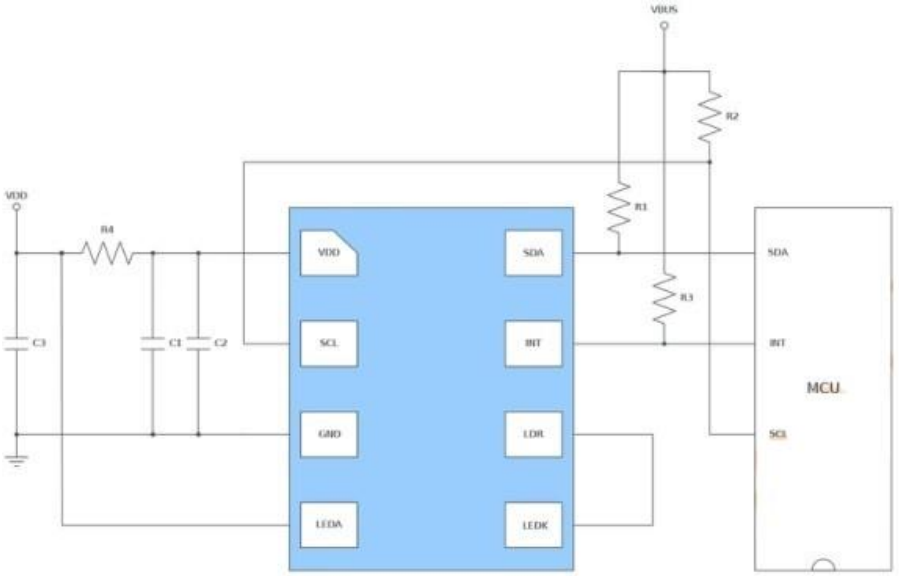
I²C General Call Software Reset

Following a General Call, (0000 0000), sending 0000 0110 (06h) as the second byte causes software reset. This feature is optional and not all devices will respond to this command. On receiving this 2-byte sequence, all devices designed to respond to the general call address will reset and take in the programmable part of their address.

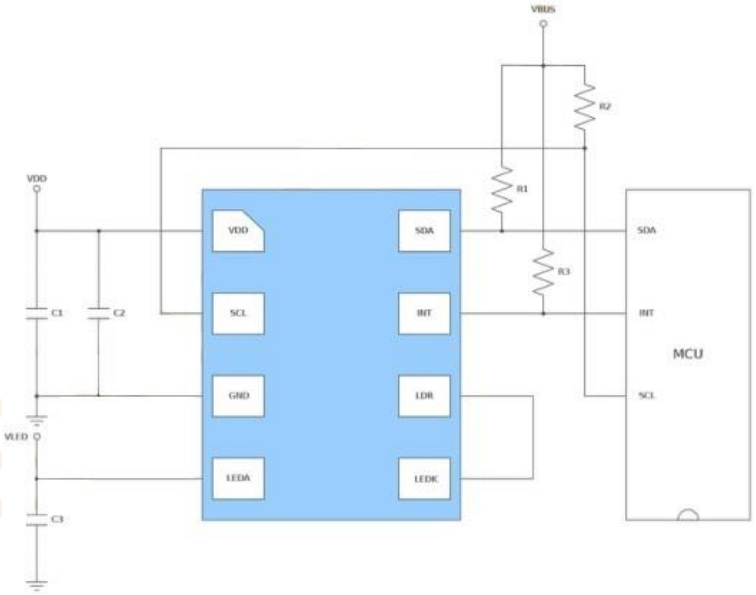
Precautions have to be taken to ensure that a device is not pulling down the SDA or SCL line after applying the supply voltage, since these low levels would block the bus.

Application Circuit

Single Power Supplies



Separate Power Supplies



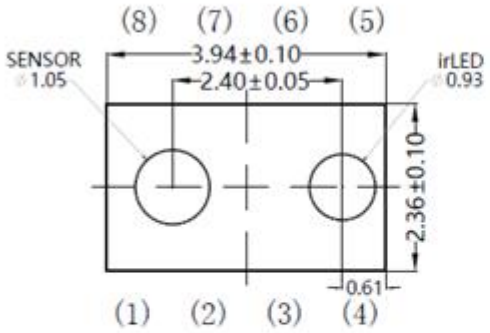
The capacitors (C1, C2) are required for sensor power supply. The capacitors should be placed as close as possible to the device. The high frequency AC noises can be shunted to the ground by the capacitors. The transient current caused by digital circuit switching also can be handled by the capacitors. A typical value 0.1 / 1 μF can be used.

The capacitors (C3) is required for LED power supply. A typical value 2.2μF is used. The extra resistor (R4) is required when using single power supply. A typical value 22Ω is used.

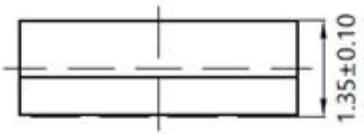
The pull-up resistors (R1, R2) are required for I^2C communication. At fast speed mode (400kHz/s) and VBUS = 3V, 1.5kΩ resistors can be used. The pull-up resistor (R3) is also required for the interrupt, a typical value between 10 kΩ and 100 kΩ can be used.

Package Outline Drawing

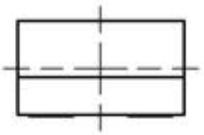
Top View



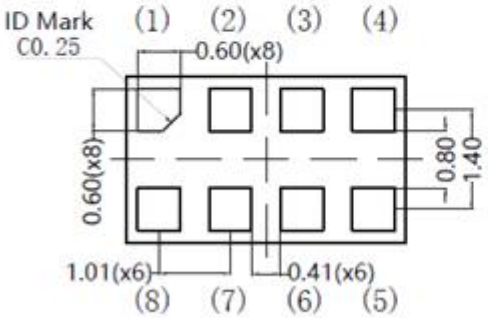
Front View



Right Side View

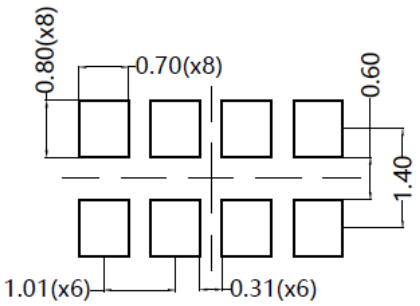


Bottom View



Pin-out	Name
(1)	VDD
(2)	SCL
(3)	GND
(4)	LEDA
(5)	LEDK
(6)	LDR
(7)	INT
(8)	SDA

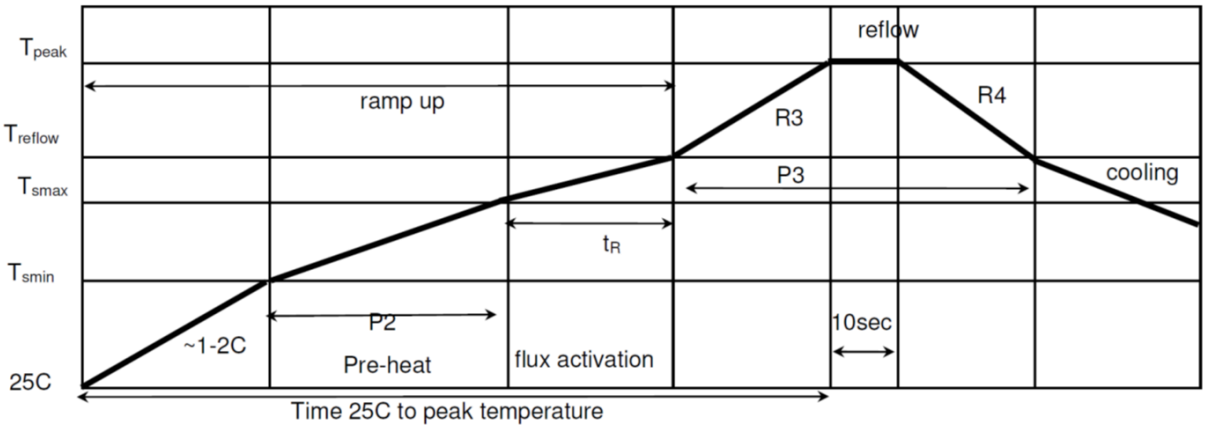
Recommended Land Pattern



Notes :

1. All dimensions in millimeters.
2. Dimension tolerance is ± 0.1mm unless otherwise noted.

Recommended Reflow Profile



	Peak temperature (Tpeak)	255-260C (max) ; 10sec
Pre-Heat	Temperature min (Tsmin) Temperature max (Tsmax) P2: (Ts min to Ts max)	150C 2C/sec 150C-217C 100s to 180s 90-110s
Time maintain above	Temperature (T_{reflow}) Time (P3) R3 slope (from 217C -> peak) R4 slope (from peak -> 217C)	217C 60-90sec 2C/sec [typ] -> 2.5C/sec (max) -1.5C/sec [typ]-> -4C/sec (max)
	Time to peak temperature	480s max
	Cooling down slope (peak to 217C)	2-4C/ sec